

Fig. 1

000001 2436260

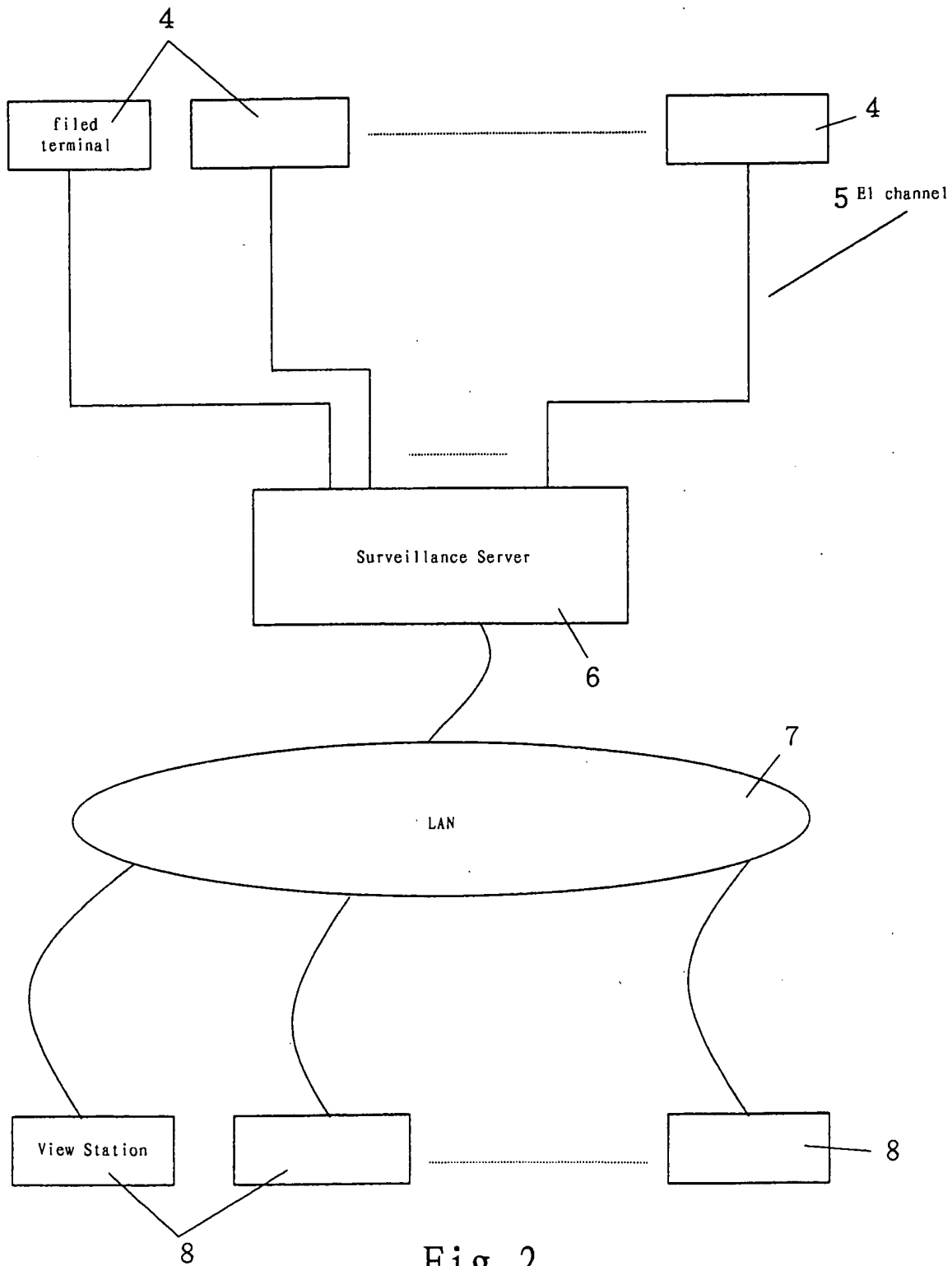


Fig. 2

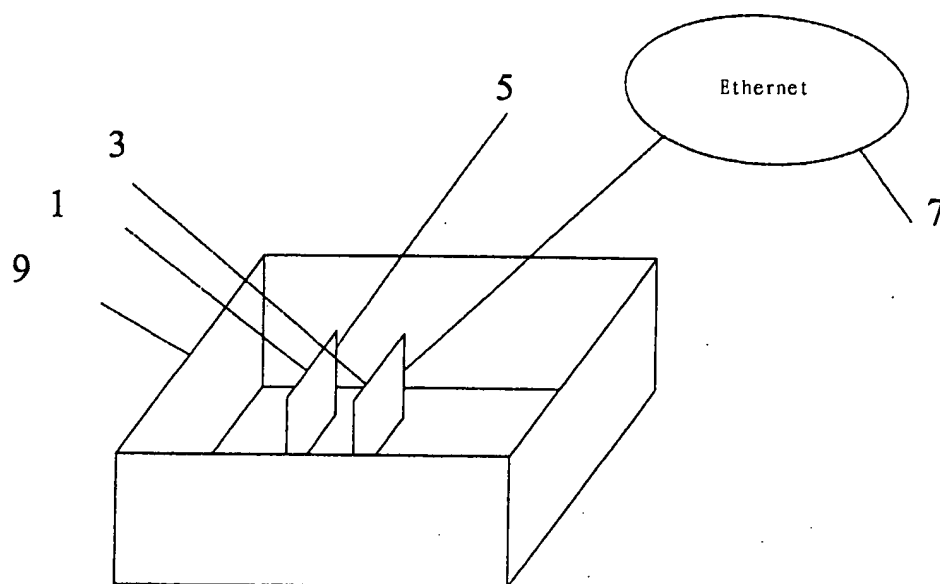


Fig. 3.

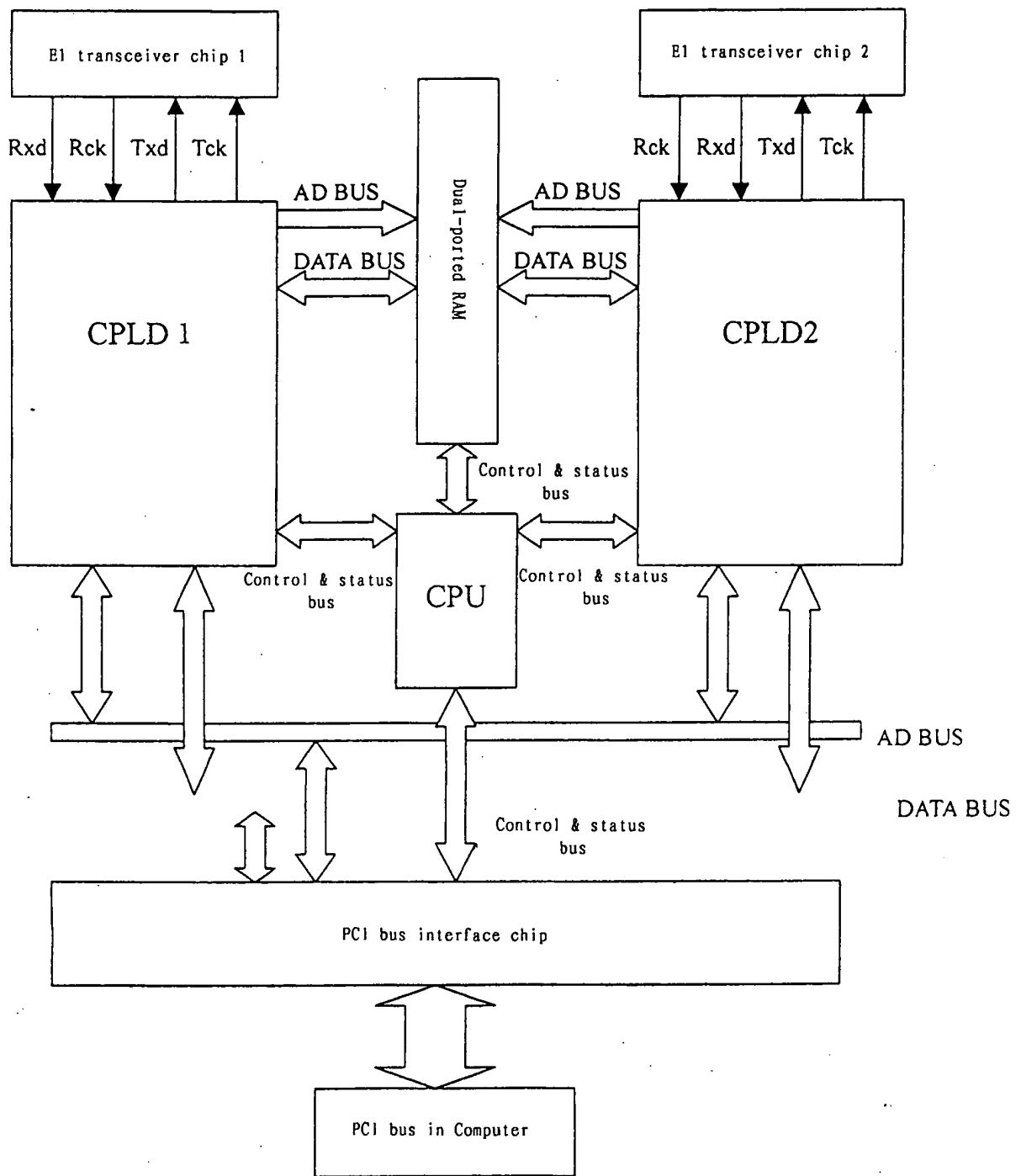


Fig. 4

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graph TD
    A[Write data to PCI bus by information process kernel] --> B[Map address on PCI bus to internal bus of board by address mapping register]
    B --> C[Request for internal bus]
    C --> D{Is internal bus idle?}
    D -- No --> C
    D -- Yes --> E[Store data into dual-ported RAM]
    E --> F[Read data from memory unit and obtain from the data channel number of field terminal to be transmitted to by CPLD]
    F --> G[Transmit data to corresponding E1 channel]
    G --> H[Complete the transmission]
  
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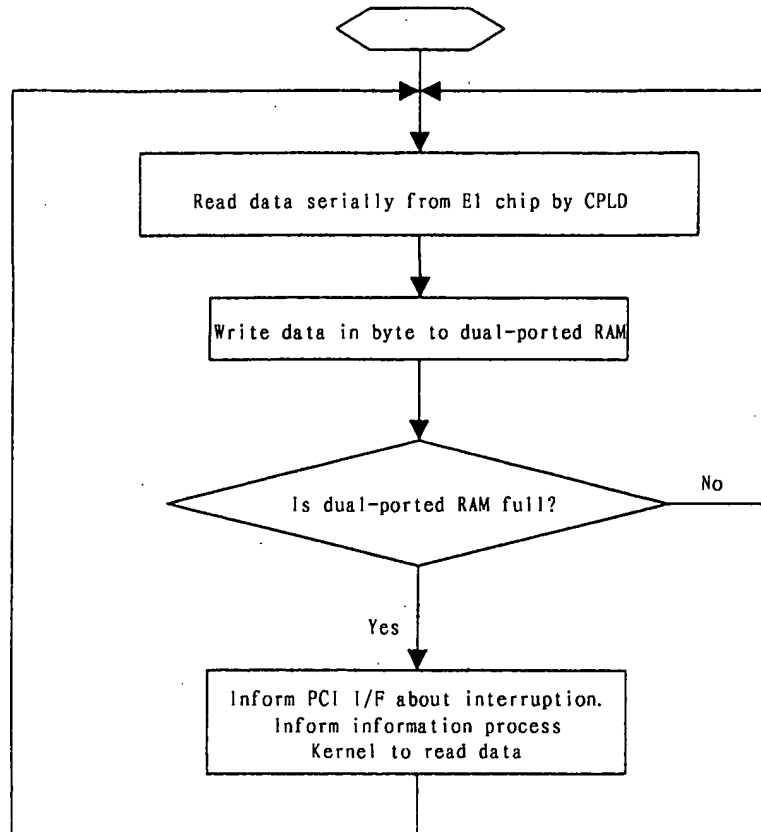


Fig. 6

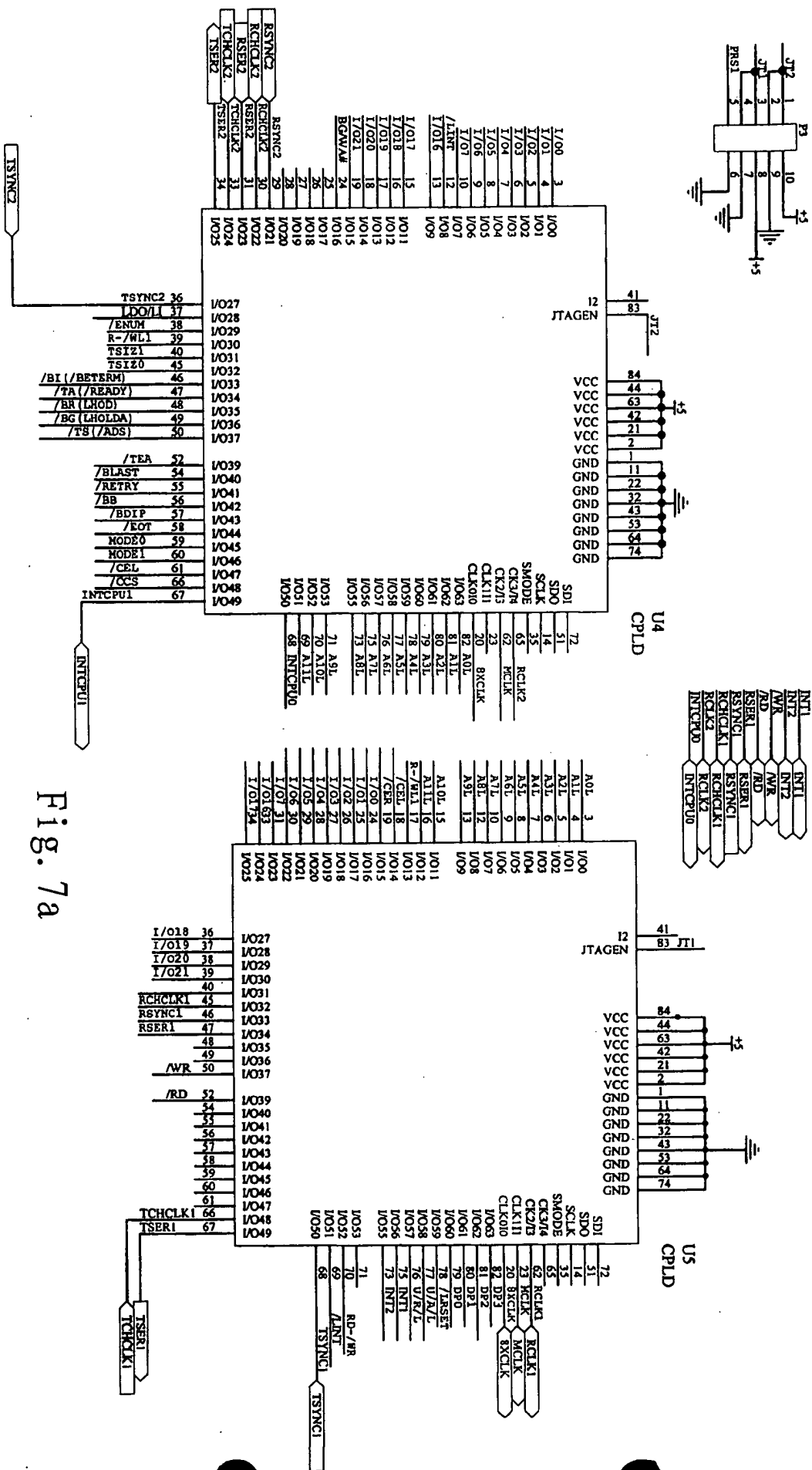
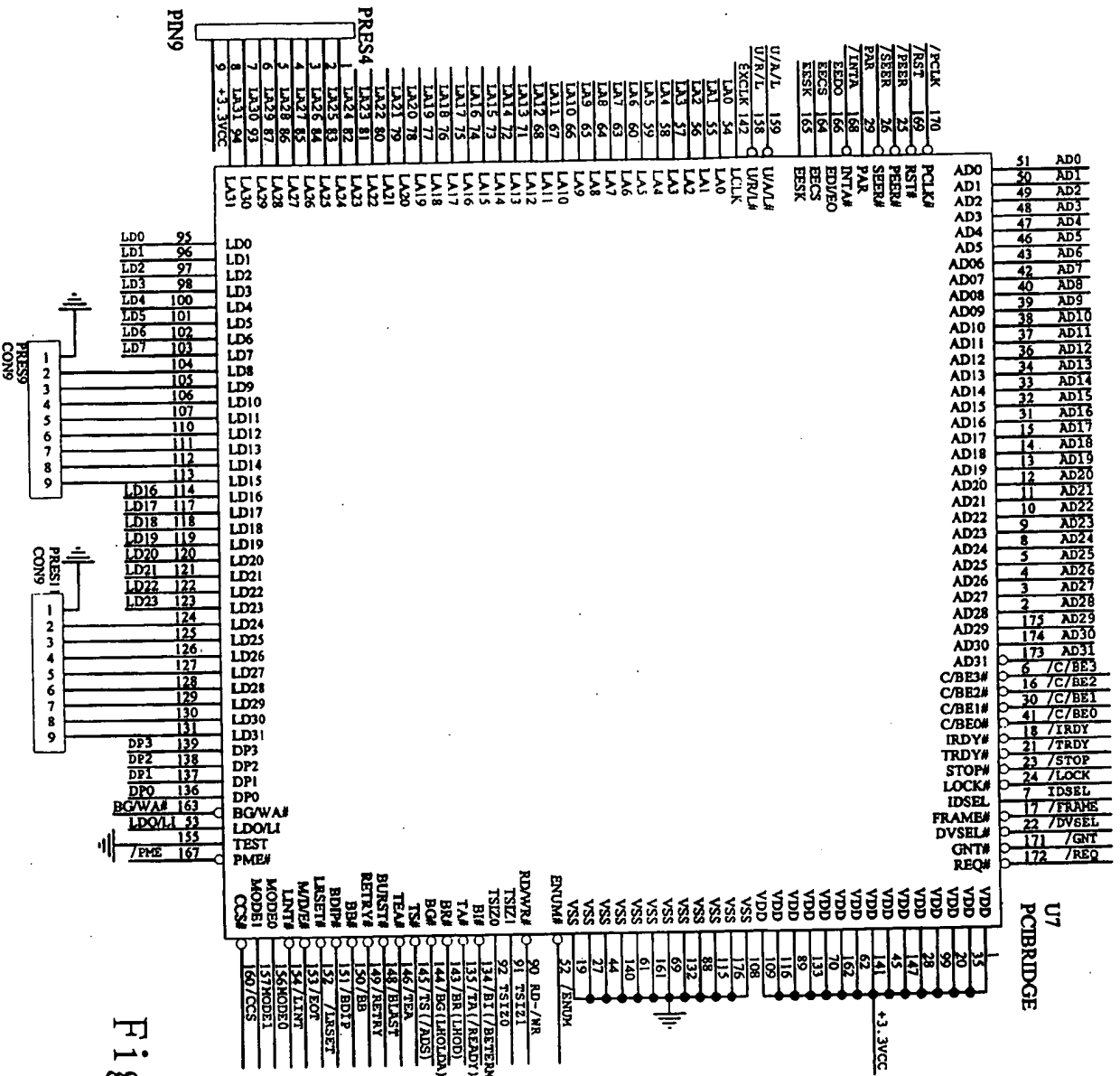


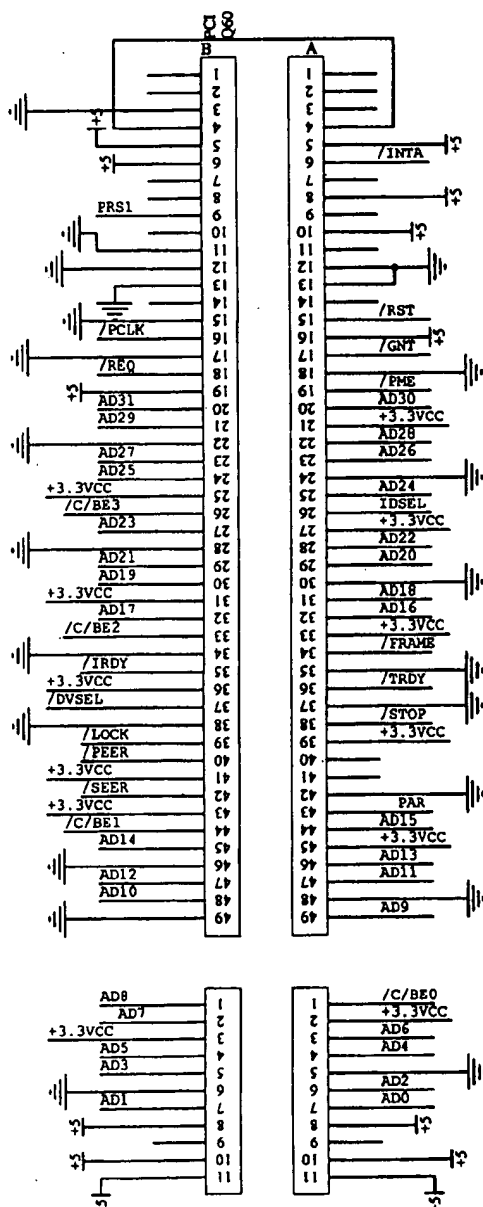
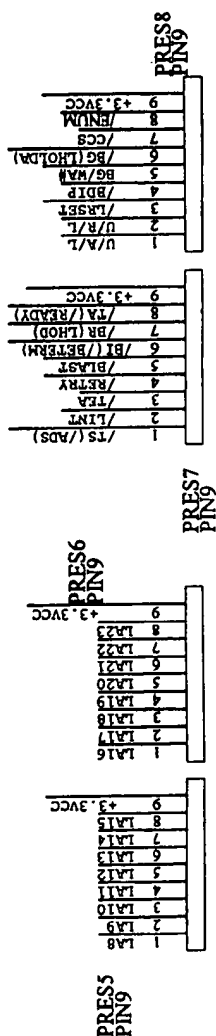
Fig. 7a





[illegible]

Fig. 7C



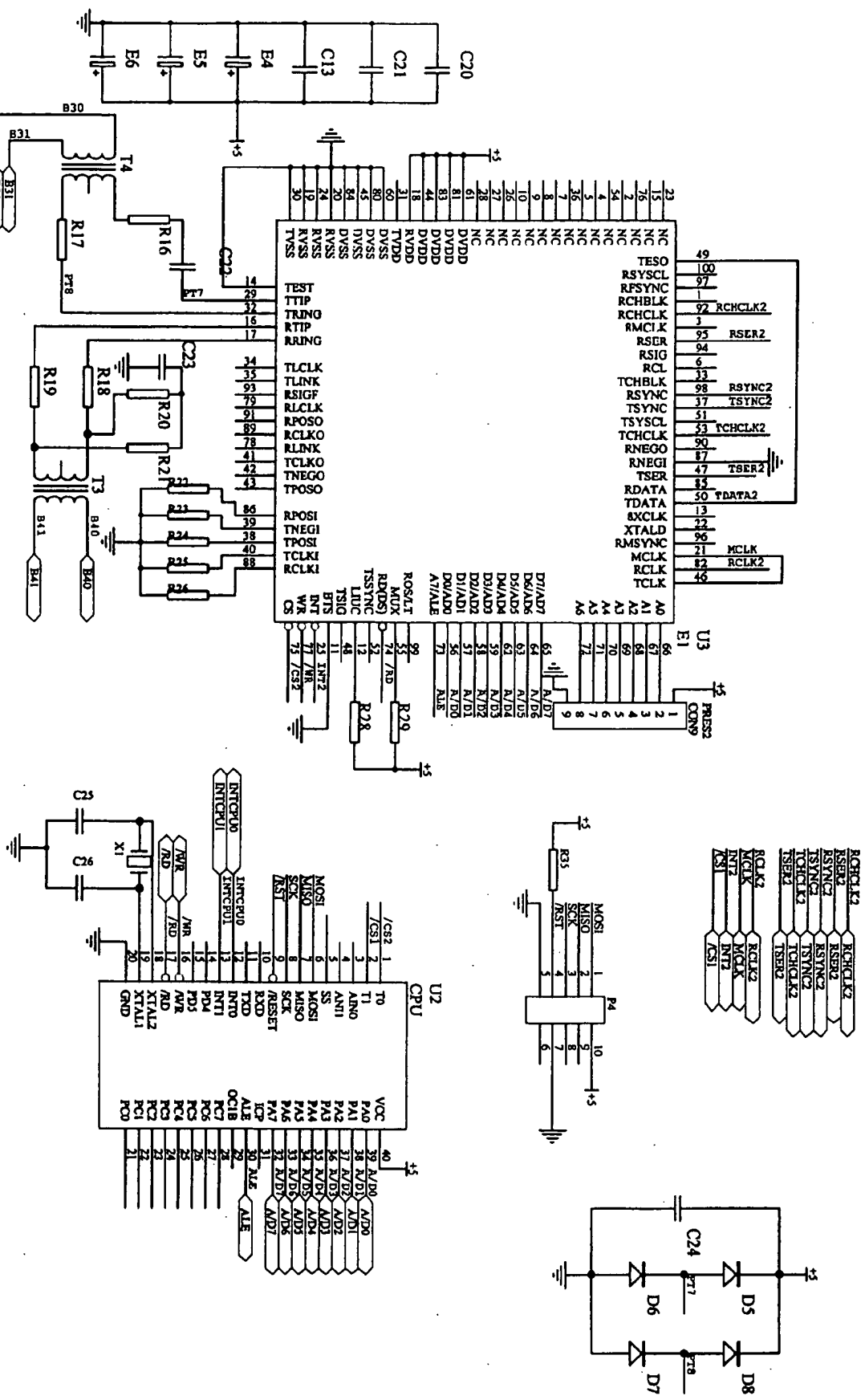


Fig. 8

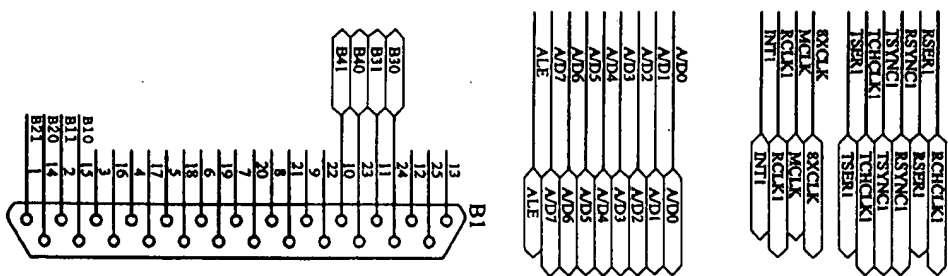


Fig. 9